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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/851,277	05/08/2001	Tae-Sung Jung	5649-894	3420

20792 7590 05/18/2004

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EXAMINER	
FLEMING, FRITZ M	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/851,277	JUNG ET AL.	
	Examiner	Art Unit	
	Fritz M Fleming	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/08/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 21,23,24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suh in view of Tsern et al. (Tsern).

In Suh, note in Figure 1 how a channel line 12 coupled to a Vtt via Rtt connects a open drain NMOS driver/transmitter 11 to a receiver 13, which receiver is in the form of a comparator, wherein comparators are usually constructed from differential amplifier circuits, due to the ability to compare an input data signal on the line 12 against a reference (i.e. 14) in order to generate an output. Note that the Figure 1 circuit is described to be a conventional memory interface such as a GTL interface or a RSL interface, but does not specifically mention that line 12 couples a memory to a memory controller.

Tsern in the same field of endeavor show how a controller 12 is coupled to a memory 16 via a BusData 18 in turn coupled to a VTERM via a resistor in a RAMBUS system (i.e. RSL).

Therefore it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify Suh by the teachings of Tsern, as Tsern has shown that the intent of the RSL interface of Suh is to couple a controller to a memory in a RAMBUS (i.e. RSL) system.

5. Claims 22,1,10,11,20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suh in view of Tsern as applied to claims 21,23,24 above, and further in view of Merritt.

Suh in view of Tsern lack the claim 22 level shifter coupling the line to the receiver.

In the same field of endeavor, Merritt shows that it is old and well known in the art to couple a level shifter 10 to couple a DRAM 100 to a controller 200, wherein 100

and 200 contain independent power supplies 30 and 230, respectively, operating at different power supply levels. For example, DRAM operates with a 2.5V VCC1 and controller 200 operates with a VCC2 of 1.8V, wherein VCC1 and 2 may be any two voltage levels, per columns 3 and 4. Thus the purpose of the level shifter is to eliminate skew (column 6).

Therefore it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the combined teachings of Suh in view of Tsern by the teachings of Merritt for the express purpose of eliminating skew when the controller and memory operate on different and independent power supply voltages. The combination is further proper, noting that Merritt uses a DRAM, as does Tsern and Suh. Thus the combined references teach the solution to skew elimination due to differing controller and memory voltage levels. As far as claims 1 and 11 are concerned, it is to be noted that Merritt applied to Suh and Tsern show that the controller and memory operate with differing and independent voltage supplies. It is to be noted in Suh that the reference voltage is generated outside of the chip (col. 2, lines 1-26), wherein the reference voltage is based upon the same Vtt that is applied to the line 12. Thus it is taught that the Vtt applied to the line 12 is external to the chip, and thus independent of the power source which supplies the receiver chip. Thus the teachings, all combined, result in three independent power supplies, one for the controller, one for the line, and one for the memory itself. As far as claims 11 and 20 are concerned, all that is required is that the terminal voltage (i.e. the Vtt or VTERM) be greater in magnitude that either of the controller or memory voltage. Such is taught by

Merritt which suggests that the controller voltage can be 1.8V and the memory voltage be 2.5V, wherein Suh suggests that the Vtt be also on the order of 2.5V. Thus in the normal course of events, either by design or fluctuation, the Vtt can exceed the memory level, as all voltages are independent of each other. Ultimate voltages are a result of the overall voltages selected, as Merritt suggests numerous voltages per column 6. Thus the selection of Vtt or VTERM to exceed the levels of the controller or memory voltage is fairly taught in the context of the overall independence of voltages.

6. Claims 2-9 and 12-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suh, Tsern and Merritt as applied to claims 1,10,11,20-24 above, and further in view of Adachi.

Suh, Tsern and Merritt teach the use of a level shifted line responsive to Vtt in a line coupling a controller to a memory. The combined references teach a single line coupling a controller to a memory via a transmitter and receiver/comparator. What is lack are two lines performing the coupling.

In the same field of endeavor, Adachi teaches a two line level shifted coupling approach for the memory 14 and controller 10. The two lines involve a transmitter 21a coupled to the receiver 25a and a transmitter 25b coupled to the receiver 21b, involving a memory 14 with a transmitter and receiver (21a,b) and a controller with a transmitter and receiver (25b,a). The purpose of this arrangement is consistent with that of Merritt, that being the ability to couple a memory to a controller in which differing supply voltages are used.

Therefore it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify Suh, Tsern and Merritt by the teachings of Adachi so as to be able to accommodate a dual line level shifted coupling between a memory and controller operating at differing and independent levels. When combined per the explicit teachings, the memory supplies its receiver and the controller supplies its receiver (i.e. per Merritt and Adachi) with the transmitters of each being in the form of the voltage independent open drain NMOS of Suh (Suh shows the transmitter coupled to the line 12 itself, thereby creating operable independence). Adachi shows the use of two level shifters, one at each end of the memory to controller coupling. Receivers have been shown to be comparators and hence differential amplifiers per Suh, with attendant reference voltages for comparison with the incoming data signal(s). Merritt teaches the use of a signal comparator (i.e. 15) in conjunction with the level shifter.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Keeth teaches a VTERM with a buffer. Taguchi teaches Vtt with a driver and comparator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz M Fleming whose telephone number is 703-308-1483. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703-308-1483. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fritz M Fleming
Primary Examiner
Art Unit 2182

fmf